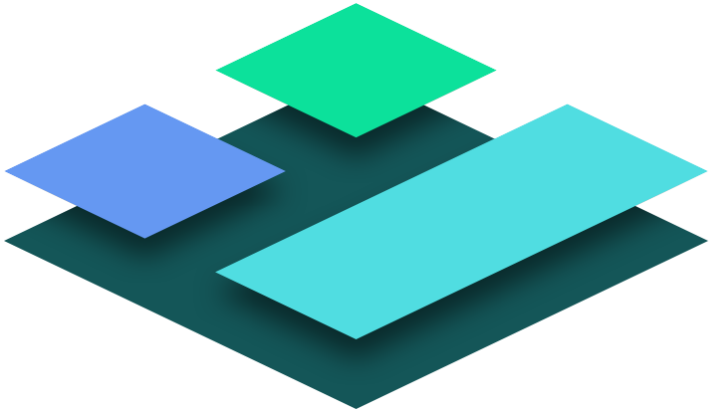


USR ALLIANCE

Nov 2017

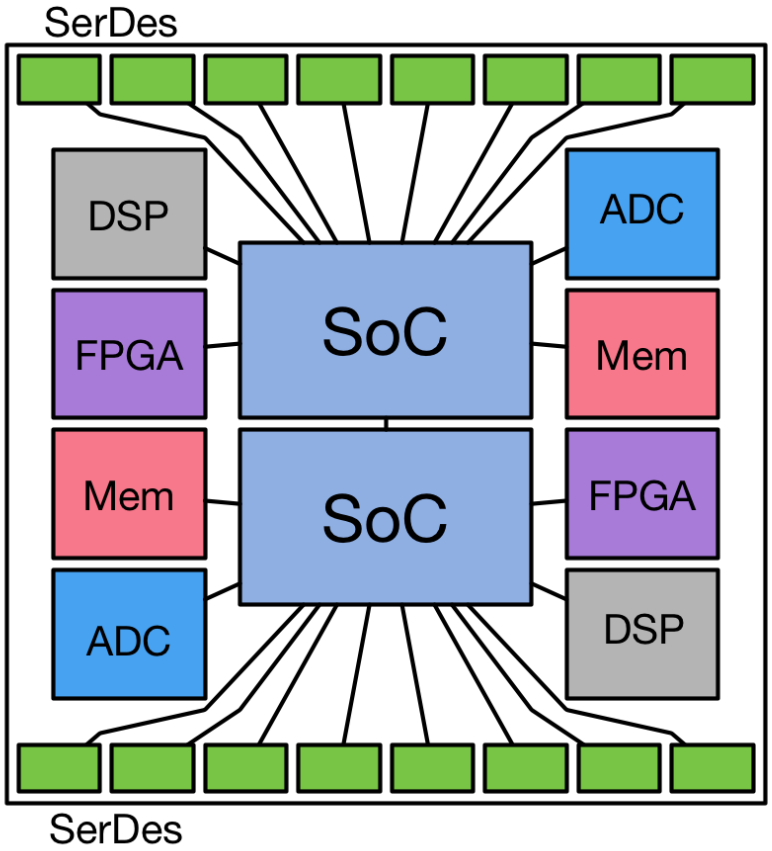
Introduction

Problem Statement

- The new silicon economy dictates different geometries and different fabrication optimizations for each silicon IP
- Monolithic approach forces all IP blocks to a single fabrication process, creating large, low yield devices
- Modular approach separates functional blocks and allows optimal process selection for each IP block
  - Allows mix-and-match of units from different semiconductor processes and sources
- Modular approach optimally uses high speed, low power Ultra-Short-Reach interconnects and Multi-Chip Modules (MCMs)
  - Use less power than XSR/VSR/MR/LR interfaces

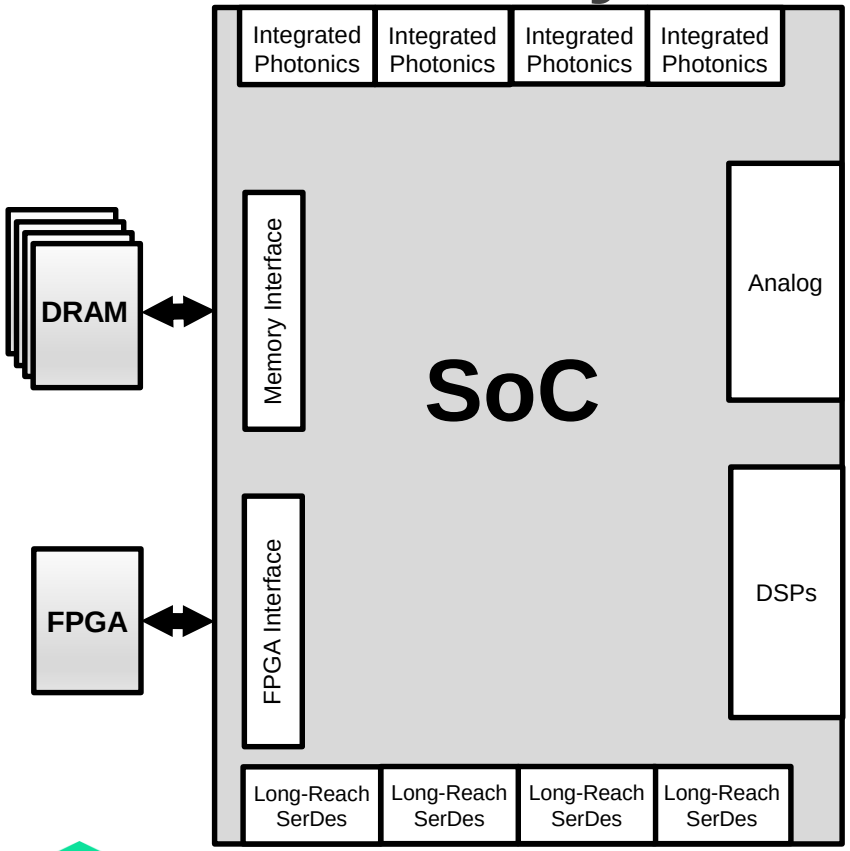
What is a USR link?

- Ultra Short Reach Link is an efficient & low power interconnect within a Multi-Chip Module (MCM) and other low-loss interconnects
  - Typically 2.5 cm or shorter
  - Can tolerate routing bends and reach the corner of the MCM
  - Low power and high bandwidth interconnect



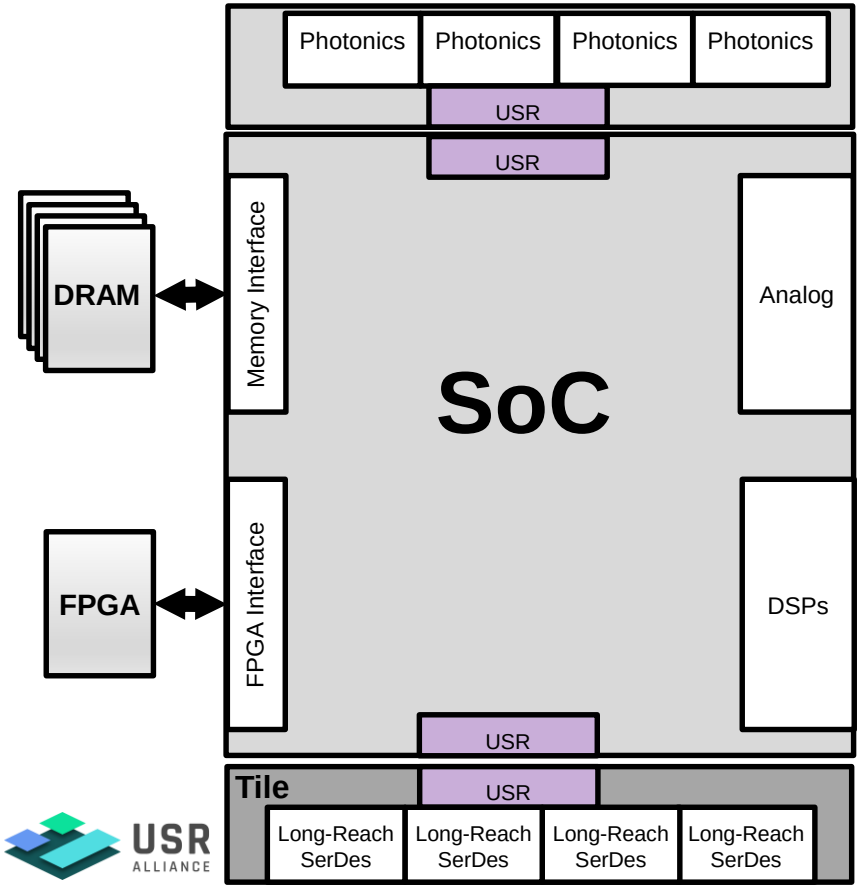
USR links – The key to Modular Solutions

Monolithic System-On-a-Chip (SoC)



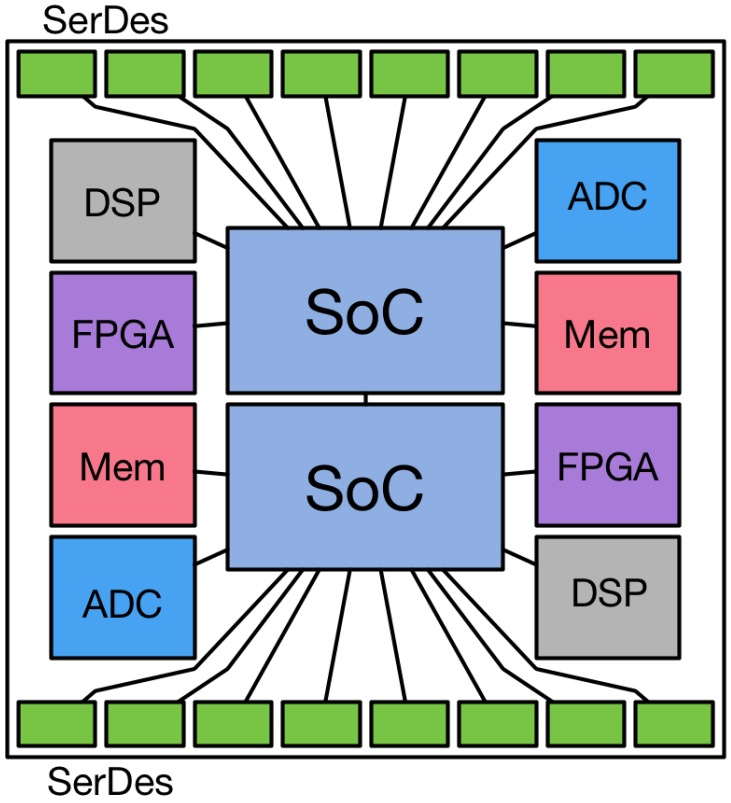
- **Integrates everything on the same silicon**
- IP block availability may lag logic process availability - Risk/schedule impact
- Analog and DSP blocks evolve at different rate as the logic – Little benefit of porting to latest process
- Integrated Photonics drive cost and add process restrictions
- Memory interfaces require substantial beachfront and often require silicon interposers for interconnect
- SoC designs are approaching yield and/or reticle size limits of the silicon technology.

Modular SerDes

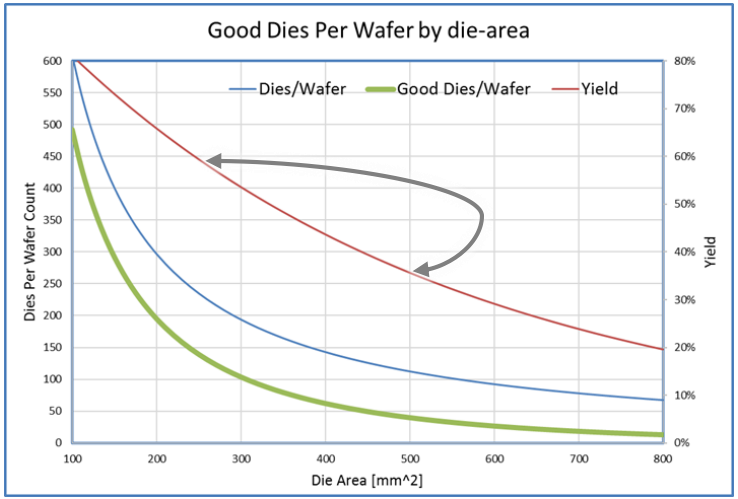


- **Move SerDes, PCS & FEC logic onto separate SerDes tile chip.**
- Allows use of SerDes in other technologies, decoupling schedule, FAB, process selection and availability dependencies
- SerDes IP is more mature on existing process, so risk and cost are reduced
- Area & power advantages for porting SerDes IP to latest technology are typically marginal
- Optimizes cost, risk & schedule

Fully Modular SoC



- Partitioning the SoC improves yields and reduces costs
- Dramatic effect when splitting an SoC with marginal yield



MCM with USR Vs. Alternatives

Parameter	MCM using USR	2.5D interposers	FO-WLP, FO-PLP
Die placement	Flexible, as of the 2.5cm USR links	Non-flexible. Strict design rules as of length of routes	Non-flexible. Strict design rules of the length of routes
Signal integrity of external interfaces	External interface can be located closer to the package balls (improving signal integrity on high speed interface)	Die location may cause long traces of external high speed interfaces. Higher resistance, impacting link performance	Die location may cause long traces of external high speed interfaces. Higher resistance, impacting link performance
Assembly Yield	Widely used technology with good yield	Specialized implementation with yield issues	Relatively new technology especially for large devices and multi dies (>2)
Number of Dies	Number of dies limited only by package size	Restriction on the number of dies assembled	Restriction on the number of dies assembled and on total silicon area
Supply chain	Multiple OSATs	Specialized suppliers	Limited number of suppliers

The USR Alliance

Goals of the USR Alliance

- Promote an efficient link, protocol & software solutions for USR applications
- Promote the development of ecosystems around USR applications
- Educate the market about USR applications
- Develop USR interoperability agreements in concert with the industry and other standards development organizations
- Create certification programs for the USR components to validate interoperability

Membership Levels

- Three participation levels: Promoter, Contributor & Adopter

	Promoter	Contributor	Adopter
Eligible for Board of Director seat	X	X[1]	
Approval of Alliance Specifications	Via Board	Via Board	
Participate & vote in Work Groups	X	X	
Chair Work Groups[2]	X	X	
Listed as Participant on web site	X	X	X
Access to final specifications and additional info and activities e.g. plug-fests	X	X	X
Included in any RAND patent guarantees	X	X	X
Cost	$20K	$10K	$5K/$1K small

[1] One seat reserved for the Contributors Group
[2] Subject to Board appointment

Policies

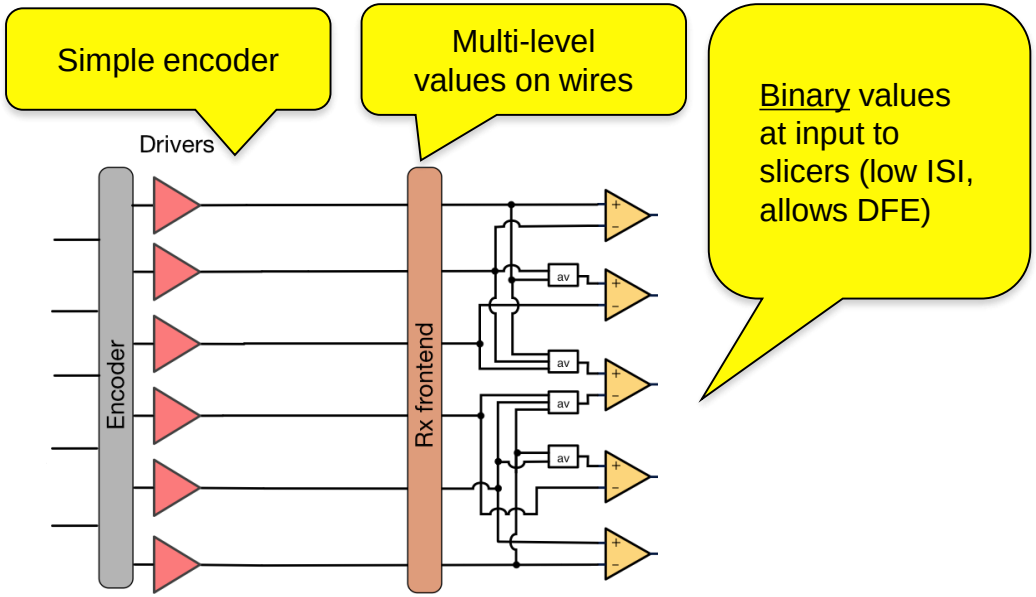
- With their permission, the USR Alliance has adopted the IP policy of the IEEE-SA with only a handful of appropriate changes (details available)
  - This policy is RAND-based (Reasonable And Non-Discriminatory)
  - The USR-Alliance RAND guarantees are available to members
    - Adopter and contributor memberships automatically available
  - Members provide RAND patent licenses on a per-application basis
- Parliamentary procedures & transparent decision-making
- Documents free to members

Possible Early USR Alliance Projects

Alliance Initial Projects

- The Alliance has four initial projects in progress:
  - Two electrical specification projects
    - 56G generation – 25 GBaud specification
    - 112G generation – extended reach specification
  - Two transport layer specification projects
    - Frame aware transport layer specification
    - Clock-and-bit transparent specification

Ideas – Make a CNRZ-5-EE PHY spec.



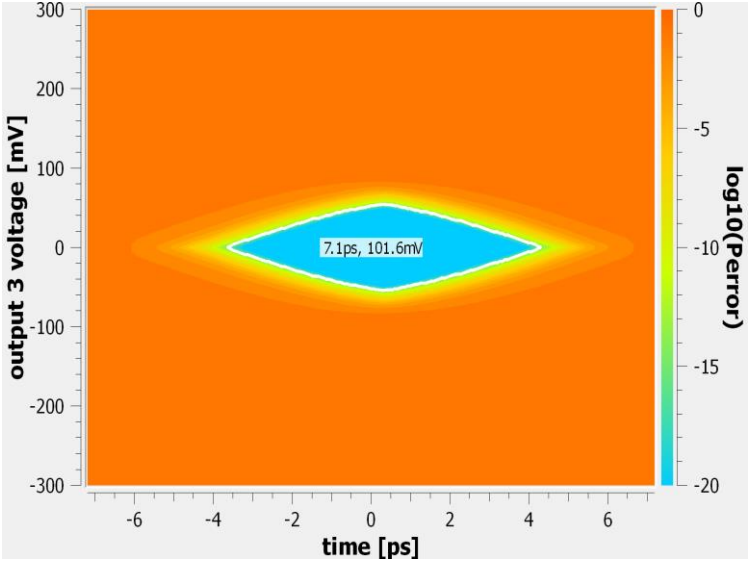
- 5 bits on 6 wires
- 5 comparators: Each compares average of 1-3 wires against another 1-3 wires
- A variant of the version defined in JEDEC JESD247

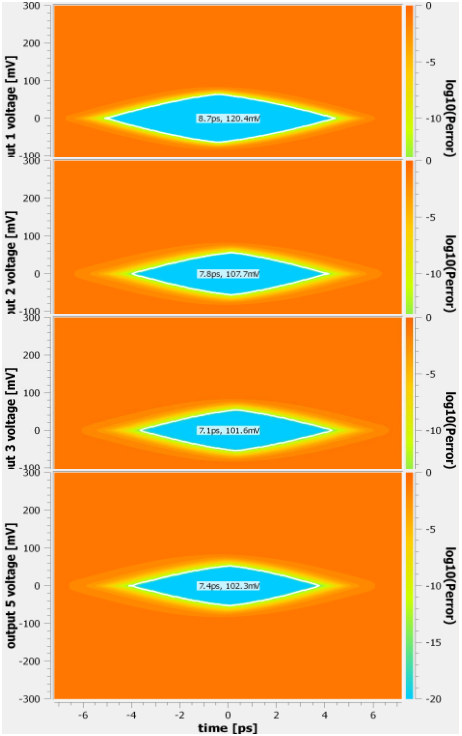
- Ideal for die-to-die interconnect inside a package
- Equal-eye code that is densely routable
  - Code has better SNR, which lowers solution power consumption
  - Code has balanced dual symmetrical triads that reduce SSO noise & EMI
- Reference-less comparators tolerate common mode noise, similar to differential
- Values at slicers are binary
  - Similar to NRZ signaling
  - ISI Ratio = 1

Ideas – Make an extended reach CNRZ-5 PHY spec. for the 100G generation

- Simulation over a 1 cm MCM link at 69.6 GBaud
  - Robust, even at high speed
  - Much larger eyes than equivalent PAM-4 solution

Smallest of the 5 eyes





Questions?